AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to FIGURE 1 that include the addition of reference numerals --10-- and --101--.

REMARKS

Objections to Specification and the Drawings

The Examiner has objected to the specification and the drawings noting that reference numerals 10 and 101 as recited in the specification are not shown in the drawings. Applicants have submitted a replacement sheet containing an amended FIGURE 1. The new FIGURE 1 includes reference numerals 10 and 101. Applicants request the Examiner to withdraw the objections to the specification and drawings.

Rejection under 35 U.S.C. § 102(e)

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,675,324 to Marisetty et al. (hereinafter Marisetty).

It is well settled that to anticipate a claim, the reference must teach every element of the claim. *See* MPEP § 2131. Moreover, in order for a reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim." *See* MPEP § 2131, citing *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990). Furthermore, in order for a reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *See* MPEP § 2131, citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913 (Fed. Cir. 1989). Applicants respectfully assert that the cited reference does not satisfy these requirements.

Claim 1 recites:

> (a) reaching a first rendezvous state;
> (b) delaying to allow other cells of said portion to reach said initial rendezvous state; and
> (c) transitioning to a second rendezvous state;
> wherein cells of said portion independently execute steps (a) through (c) in parallel.

Claim 12 is directed to a cell for use in a multi partition computer system that comprises:

> processor to execute said partition instructions;
> firmware device to store said partition instructions;

code to set a register reflecting a first rendezvous state;
code to delay partition formation operations after setting said register to reflect said first rendezvous state; and
code to transition to a second rendezvous state after delaying partition formation operations.

Marisetty is directed to a multi-processor system that involves an error handling routing. When an error occurs (a parity error associated with the processor instruction cache), one of the processors is selected to execute an error handling routine defined in system firmware. The error handling routine causes the system to enter a rendezvous state. In the rendezvous state, one of the processors acts as a "monarch processor" to attempt to correct the error. Col. 5, lines 48-50. The other processors enter a "spin-loop" or "idle state" Col. 6, lines 60-65. After correction of the error by the monarch processor, the system "exits the rendezvous state and all processors resume normal operations." Col. 5, lines 51-53.

As explicitly described by Marisetty, the error handling procedure only involves a single rendezvous state and, upon completion of the error handling routine, the rendezvous state is exited. Accordingly, Marisetty does not disclose transitioning to "a second rendezvous state" in the manner recited by claims 1 and 12.

Applicants respectfully submit that Marisetty does not disclose each and every limitation of claims 1 and 12. Claims 2-11 and 13-20 depend from base claims 1 and 12 respectively and, hence, inherit all limitations of their base claim. Accordingly, Applicants respectfully submit that Marisetty does not anticipate claims 1-20.

New Claims

Applicants have added new claims 21-27. New claims 21-27 are supported by the original application. No new matter has been entered.

Claim 21 recites:

transitioning to a partition formation state, by each cell, at the earliest of (i) an expiration of a timer, (ii) all cells, within the same partition as indicated in said configuration data, setting their respective registers, and (iii) another cell within the same partition indicating transition to said partition formation state;...
forming partitions using common information in said local partition sets.

Applicants respectfully submit that the cited reference does not teach or suggest each and every limitation of claim 21. For example, Marisetty is merely directed to an error handling procedure in a multi-processor computer system. However, there is no disclosure of partitions in Marisetty. Accordingly, Marisetty does not teach or suggest transitioning to a partition formation state in the manner recited by claim 21 or forming partitions in the manner recited by claim 21.

Applicants respectfully submit that claim 21 is patentable over Marisetty. Claims 22-27 depend from claim 21 and, hence, inherit all limitations of claim 21. Accordingly, claims 22-27 are patentable over Marisetty by depending from an allowable base claim in addition to the novel and nonobvious limitations recited therein.

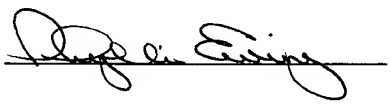
Conclusion

In view of the above, Applicants believe the pending application is in condition for allowance. Applicants believe a fee of $350.00 is due with this response. However, if an additional fee is due, or for any overpayment, please charge/credit Deposit Account No. 08-2025, under Order No. 10001626-1 from which the undersigned is authorized to draw.

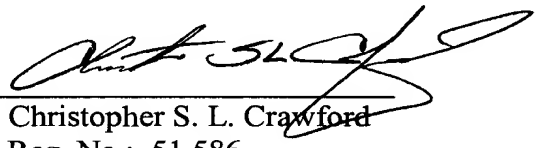
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482738697US, in an envelope addressed to: MS Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Date of Deposit: December 21, 2004

Typed Name: Phyllis Ewing

Signature: 

Respectfully submitted,

By 

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Date: December 21, 2004